REMARKS

Claims 1-7 and 9-24 are presented for examination, of which claims 1, 12, 19 and 23 are in independent form.

Claims 1, 12, 19 and 23 are amended by the present response. Additionally, claim 8 is cancelled without prejudice, limitation, waiver or estoppel, its subject matter being incorporated into base claim 1, and claim 24 is added.

Support for the amendments may be found in the present patent application, for example, in respect of FIGS. 3 and 5A-5E and the associated description at Paragraphs **[0018]**, **[0022]** and **[0024] - [0028]**, *inter alia*.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Specification

In the pending Office Action, the specification is objected to for certain informalities. Applicant has appropriately amended the specification by way of the present response. It is therefore believed that the pending objections to the specification have been overcome or otherwise rendered moot.

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PATENT APPLICATION
DOCKET NO.: 200300031-2

Regarding the Claim Rejections - 35 U.S.C. §103(a)

In the pending Office Action, claims 1, 3, 5 and 9-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,084,934 to Garcia et al. (hereinafter the *Garcia* reference) in view of U.S. Patent No. 6,317,806 to Audityan et al. (hereinafter the *Audityan* reference).

Additionally, claims 2, 4, 6 and 7 are each rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of the *Garcia* reference and the *Audityan* reference with various other references, i.e., U.S. Patent No. 6,249,875 to Warren, U.S. Patent No. 6,115,823 to Velasco et al. and U.S. Patent Application No. 20030016697 to Jordan.

In connection with these rejections, the Examiner has commented as follows with regard to claim 1:

> Regarding claim 1, Garcia discloses a system for effectuating the transfer of data blocks having intervals across a clock boundary between a first clock domain and a second clock domain (Abstract, 1st 4 lines; column 1, lines 6–9; Fig. 1, element 14 clock rate CLK Y and element 12 at clock rate CLK X), wherein said first clock domain is operable with a first clock signal and said second clock domain is operable with a second clock signal (Figs. 1 & 2, CLK Y and CLK X), said first and second clock signals having a ratio of N first clock cycles to M second clock cycles, wherein N/M>1 (Fig. 4, CLK Y comprising 9 clock

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cycles to CLK X comprising 8 clock cycles; wherein N=9 and M=8), comprising:

a first circuit portion for providing said data blocks to a second circuit portion (Fig. 2, elements 14 and 12; column 2, lines 49–54; wherein the first circuit is element 14 and the second circuit is element 12);

a synchronizer controller disposed between said first and second clock domains for providing at least one dead cycle control signal to said second circuit portion, wherein said at least one dead cycle control signal is indicative of the location of at least one dead cycle between said first and second clock signal (Fig. 2, element 16; Fig. 3; Fig. 4, element HIGH STROBE; wherein the synchronizer controller is interpreted as the detection module 16 which generates the LOW STROBE and HIGH STROBE outputs and the HIGH STROBE output indicates the position of the dead cycle, as shown in Fig. 4);

whereby said data blocks are transmitted as contiguous data blocks relative to said at least one dead cycle (Fig. 4, data blocks transmitted according to HIGH STROBE).

Garcia doesn't disclose control logic for generating data transfer control signals.

In the same field of endeavor, however, Audityan discloses control logic associated with said second circuit portion for generating data transfer control signals responsive to said at least one dead cycle control signal, said data transfer control signals for controlling said second circuit portion (Fig. 1, element 51 output that controls the mux 19 which receives data from the queue 16; column 5, lines 25–39, 52–60; column 7, lines 17–27; wherein the control logic is interpreted as the decoder 19, the data control signals are interpreted as the output of the decoder that control the selection from the queue 16 and the

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> input to the decoder 51 is interpreted as the dead cycle control signal).
>
> Therefore it would have been obvious to one having ordinary skill in the art, at the time the invention was made, to use the method, as taught by Audityan, in the system of Garcia because this would allow the appropriate data element from the queue to be selected, as disclosed by Audityan (same column, line numbers as above).

Additionally, the Examiner has commented that claims 12 and 19 were analyzed as corresponding to limitations of claim 1, while base claim 23 was analyzed as corresponding to limitations of claim 19.

Base claim 1

Base claim 1 has been amended to incorporate the subject matter of claim 8, which the Examiner has indicated to be allowable. Accordingly, it is believed that base claim 1 is now in condition for allowance. Claims 2-7 and 9-11 depend from claim 1 and are also believed to be allowable over the art of record.

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Base claims 12, 19 and 23

Applicant respectfully submits that the pending §103(a) rejections of claims 12-23 as set forth above have been overcome or otherwise rendered moot by way of the present amendment.

As currently defined by base claim 12 an embodiment of the present disclosure is directed to a circuit for effectuating the transfer of data blocks having intervals to a synchronizer disposed between two clock domains. The claimed circuit comprises, *inter alia*, means for receiving and temporarily storing a first portion of the data blocks having intervals and means for selecting between the first portion of the data blocks and a second portion of the data blocks provided without queuing, whereby the data blocks are transmitted to the synchronizer as a packet of contiguous data blocks relative to at least one dead cycle.

Similarly, as defined by base claim 19, an embodiment of the present disclosure is directed to a method for effectuating the transfer of data blocks having intervals across a clock boundary. The method comprises, *inter alia*, generating advance notice indicative of the location of at least one dead cycle occurring

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between a first clock signal and a second clock signal used for transmitting data across a clock boundary, receiving packet data and the advance notice indicative of the location of the dead cycle, the packet data including the data blocks having intervals, calculating the optimal time to send the packet data relative to the location of said at least one dead cycle and transmitting ordered contiguous data blocks about the at least one dead cycle to a CLK1-to-CLK2 synchronizer for transmission to receive circuitry disposed in the second clock domain. Additionally, base claim 23 contains limitations substantially similar to those of base claim 19.

As discussed in the instant patent application, the claimed "data blocks having intervals", also referred to as intervaled data blocks, may include one or more bits that are spaced apart by an interval element. The interval element may include empty cycles, such as in the example, $A_0\_B_0\_C_0\_D_0$, where each "_" represents an empty cycle. The interval element may also be data blocks that have been multiplexed with the original data blocks to create interleaved data blocks, such as in the example, $A_0A_1B_0B_1C_0C_1D_0D_1$. In either example, the data is sent across the

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clock boundary as a contiguous data block. See, e.g., page 7, lines 1-16 of the application as filed.

The *Garcia* reference is directed to the transfer of data across an asynchronous clock boundary. As shown in the timing diagram of FIG. 4 of the *Garcia* reference, reproduced herein for convenience, CLK X is the clock signal of the receiver of the data, while CLK Y is the clock signal of the sender of the data. CLK X operates at a slower rate than does CLK Y, so that the receiver is not able to receive data on every clock cycle of CLK Y. To coordinate the transfer of data, the receiver generates a HIGH ENABLE signal, which is synchronized with CLK X and is provided to the sender to indicate that the receiver is able to receive data when the signal is high. The sender stages the HIGH ENABLE signal through a series of latches that are clocked by CLK Y to produce the HIGH STROBE signal shown. The

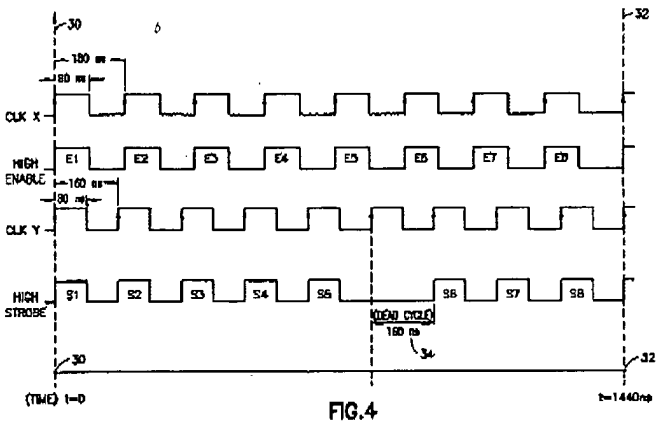

FIG.4

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sender will only send data in clock cycles in which the HIGH STROBE signal is high. When the HIGH STROBE signal is low for a clock cycle of CLK Y, a dead cycle occurs in which no data is sent. See column 4, line 50 through column 5, line 7.

While the *Garcia* reference appears to provide for the transfer of data across the clock boundary, the teachings therein do not discuss receiving data blocks having intervals and sending contiguous data blocks, as is currently recited in the claimed embodiments. Further, this reference does not disclose or suggest that the data blocks for transmission are selected from a first portion of the data blocks that are temporarily stored and a second portion of the data blocks that are provided without queuing, as is recited in the embodiment of claim 12. Additionally, *Garcia* does not disclose or suggest that there is advance notice of the location of the dead cycle, as recited in the embodiment of claims 19 and 23. The *Garcia* reference indicates the dead cycle by the lack of a pulse in the HIGH STROBE signal, as shown in the Figure above, but the dead cycle is indicated as it occurs; no advanced notice is provided or suggested.

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The *Audityan* reference does not cure the foregoing deficiencies of the *Garcia* reference. The *Audityan* reference discloses a queuing apparatus that uses multiplexers to select specific data elements in the queue. See column 5, lines 25-60. There is no disclosure or suggestion that the data blocks received have intervals, as recited in the claimed embodiments. Further, this reference does not disclose or suggest that the queuing apparatus selects between a first portion of data blocks that are temporarily stored and a second portion of data blocks that are provided without queuing, as recited in the embodiment of claim 12. Additionally, the *Audityan* reference does not disclose or suggest providing advance notice of a dead cycle, as recited in the embodiments of claims 19 and 23. Accordingly, at a minimum, the combination of the *Garcia* and *Audityan* references fails to teach or suggest all the limitations of base claims 12, 19 and 23, a prerequisite for establishing a *prima facie* case of obviousness.

Based on the foregoing, Applicant respectfully submits that base claims 12, 19 and 23 are not anticipated or suggested by the applied art of record, and are therefore in condition for

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allowance. Claims 13-18 depend from base claim 12 and introduce additional limitations therein. Likewise, claims 20-22 depend from base claim 19 and introduce additional limitations therein. Accordingly, these dependent claims are also believed to be in condition for allowance.

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SUMMARY AND CONCLUSION

In view of the fact that none of the art of the record, whether considered alone or in combination discloses, anticipates or suggests the pending claims, and in further view of the above remarks and amendments, reconsideration of the Action and allowance of the present patent application are respectfully requested and are believed to be appropriate.

Respectfully submitted,

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